

An Efficient Parallel SAT Solver Exploiting Multi-Core Environments, Phase I

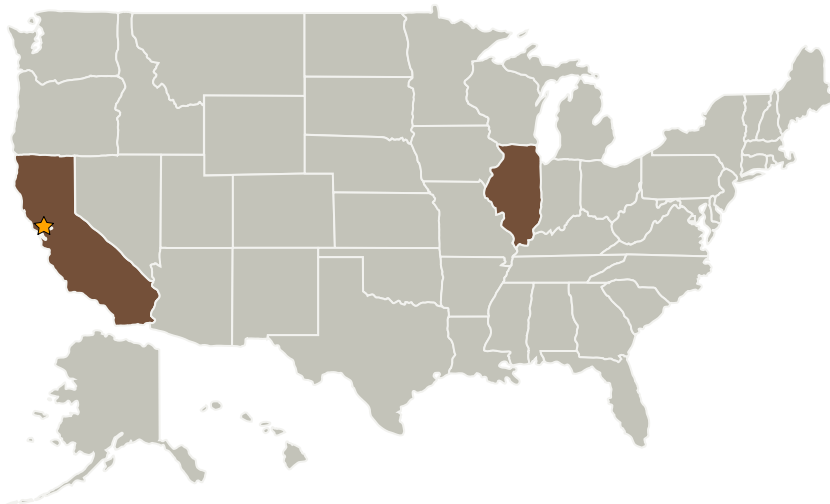
Completed Technology Project (2009 - 2009)



Project Introduction

The hundreds of stream cores in the latest graphics processors (GPUs), and the possibility to execute non-graphics computations on them, open unprecedented levels of parallelism at a very low cost. We will investigate ways to efficiently exploit this parallelism in order to accelerate the execution of a Boolean Satisfiability (SAT) solver. SAT has a wide range of applications, including formal verification and testing of software and hardware, scheduling and planning, cryptanalysis, and detection of security vulnerabilities and malicious intent. We bring a tremendous expertise in SAT solving, formal verification, and solving of Constraint Satisfaction Problems (CSPs) by efficient translation to SAT. In our previous work (done on the expenses of our company) we obtained 2 orders of magnitude speedup in solving Boolean formulas from formal verification of complex pipelined microprocessors, as well as 4 orders of magnitude speedup in SAT-based solving of CSPs. We expect to achieve speedups of up to 1 -- 2 orders of magnitude in Phase 1, and up to 3 -- 4 orders of magnitude in Phase 2.

Primary U.S. Work Locations and Key Partners



Organizations Performing Work	Role	Type	Location
★ Ames Research Center(ARC)	Lead Organization	NASA Center	Moffett Field, California
Aries Design Automation, LLC	Supporting Organization	Industry	Chicago, Illinois



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Table of Contents

Project Introduction	1
Primary U.S. Work Locations and Key Partners	1
Organizational Responsibility	1
Project Management	2
Technology Areas	2

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Center / Facility:

Ames Research Center (ARC)

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

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Primary U.S. Work Locations

California

Illinois

Project Management

Program Director:

Jason L Kessler

Program Manager:

Carlos Torrez

Technology Areas

Primary:

- TX15 Flight Vehicle Systems
 - └ TX15.1 Aerosciences
 - └ TX15.1.3 Aeroelasticity